



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

MARK ANDERS

Application No.: 10/035,574

Filed: October 18, 2001

For: **TRANSITION ENCODED DYNAMIC BUS
CIRCUIT**

Art Group: 2611

Examiner: Sudhanshu C. Pathak

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted concurrently with the Request for Continued Examination. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

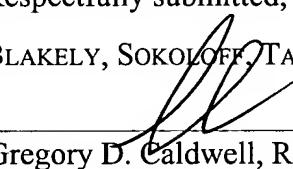
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Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: July 10, 2006



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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



Julie Dussault

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Date



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Sheet	1	of	2	Application Number	10/035,574
				Filing Date	October 18, 2001
				First Named Inventor	Mark Anders
				Art Unit	2611
				Examiner Name	Sudhanshu C. Pathak
				Attorney Docket Number	42390P11426

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

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Complete if Known

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Examiner Name	Sudhanshu C. Pathak
Attorney Docket Number	42390P11426

U.S. PATENT DOCUMENTS

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		US-6,005,417	12-21-1999	MEHTA et al.	
		US-6,028,814	02-22-2000	LIM	
		US-6,140,843	10-31-2000	HOWARD	
		US-6,188,596	02-13-2001	HOLST	
		US-6,417,698	07-09-2002	WILLIAMS et al.	
		US-6,453,399	09-17-2002	WADA	
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		US-6,741,094	05-25-2004	OGAWA	
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		US-6,990,035	01-24-2006	REDWINE et al.	
		US-2003/0001184	01-02-2003	ANDERS et al.	
		US-2003/0107411	06-12-2003	MARTIN et al.	
		US-2005/0285631	12-29-2005	GOLDMAN et al.	
		US-2006/0140034	06-29-2006	HSU et al.	
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Signature		Date Considered
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of

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Examiner Name	Sudhanshu C. Pathak
Attorney Docket Number	42390P11426

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Anders, Mark, et al., "A Transition-Encoded Dynamic Bus Technique for High-Performance Interconnects", Symposium on VLSI Circuits, Digest of Technical Papers, pp. 16-17 (Jun. 13-15, 2002).	
		Anders, Mark, et al., "A Transition-Encoded Dynamic Bus Technique for High-Performance Interconnects", IEEE Journal of Solid-State Circuits, Vol. 38, No. 5, pp. 709-714 (May 2003).	
		Stan, Mircea R., et al., "Bus-Invert Coding for Low-Power I/O", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 3, No. 1, pp. 49-58 (Mar. 1995).	

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